# Experimental analysis of above-IC inductor performance with different patterned ground shield configurations and dummy metals

X. Sun, G. Carchon, Y. Kita*, K. Chiba*, T. Tani* and W. De Raedt

IMEC, Integrated Systems Department, Kapeldreef 75, B-3001, Leuven, Belgium

* OKI Electric Industry Co. Ltd., Tokyo, Japan
xiao.sun@imec.be

***Abstract*** **— This paper presents the characterization of various patterned ground shield configurations for single ended inductor layouts: center ground shield (CGS), simple ground shield (SGS) and perimeter ground shield (PGS). Experiments and simulations show that when the shields connect only to one side of single-ended above-IC inductor RF ground pad, an asymmetric Q-behavior is obtained. HFSS simulations indicate that a better performance may be obtained by a symmetrical connection of the shield to the RF ground. Furthermore, the influence of different metal shield widths and spacings, as well as the effect of dummy metal dimensions on the performance of inductors has been assessed.**

***Index Terms*** **— Above-IC inductors, Patterned ground shield, Q-factors.**

## I. Introduction

High-Q on-chip inductors are important components for modern radio frequency integrated circuits (RFICs). However, on-chip RF inductors have fairly low Q-factors mainly because of the large series resistance associated with the thin metal layers for IC connections, conductive silicon substrate and substrate parasitic capacitances. Several approaches have been used to improve the Q factor for silicon-based integrated inductors. Previously, we have demonstrated that a high performance may be achieved for inductors realized using wafer level packaging techniques, especially when the inductors are combined with patterned ground shields [1]. The use of patterned ground shields is attractive because it does not require additional process steps in standard silicon technologies. In this paper, we will focus on the design and characterization of different patterned ground shield configurations combined with above-IC inductors: in section III we discuss how the connections between shields and inductor RF ground pad can influence the inductor performance; the shield bars width and spacing, as well as the influence of dummy metal dimensions on inductor performance will be demonstrated in section IV and V.

## II. Technology Description

The above-IC inductors have been realized above OKI 6" SOI wafer using IMEC-WLP technology [2,3]. The inductors have been realized on WLP-M1 (5μm electroplated Cu) and separated from the back-end of line (BEOL) by BCB-1 (16μm) (Fig. 1), overpasses are realized in WLP-M2 (2 μm Cu, 3μm Ni/Au) and separated from WLP-M1 by BCB-2 (8μm). In OKI SOI wafer, the patterned ground shields have been realized in metal layer T4M, 0.72μm Al. The above-IC layers have been connected to BEOL layers by a high aspect ratio via (HARVI).

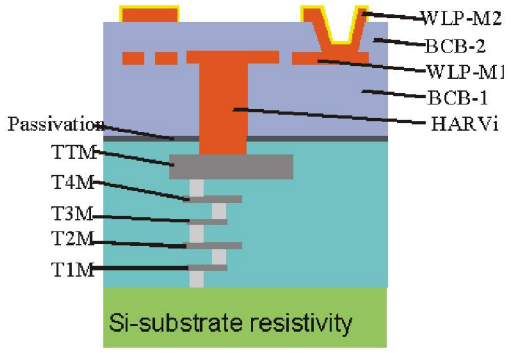



Fig. 2 Schematic cross section of the Above-IC inductor on OKI SOI wafer with BEOL layers

## III. Characterization of Various Patterned Ground Shields

Three shield configurations have been realized: perimeter ground shield (PGS) in Fig. 3, center ground shield (CGS) in Fig. 4, Fig. 5 is simple ground shield (SGS), the simplified version of center ground shield. CGS and SGS are connected to ground only by connecting to left RF ground pad, and PGS are connected in both sides. All ground pads are connected in the above-IC layers. A typical single-ended spiral inductor combined with these three shield configurations has been investigated. The number of turns of inductor is 1.5, the radius of the opening in the middle of spiral is 100μm, the width of the metal traces is 20μm, and distance between the traces is 10μm. Wafer-level two-port S-parameter measurements were made from 45MHz to 30 GHz using an HP8510C Network Analyzer. We extracted intrinsic inductance from measurements $Y_{21}$ in equation (1), rather

than from $Y_{11}$ or $Y_{22}$. This makes the extracted inductance less dependant on the parasitic capacitances.

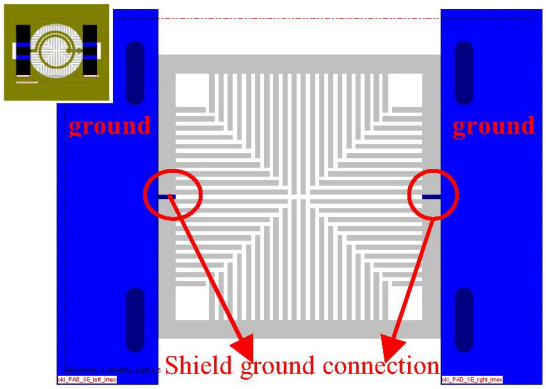



Fig. 3 Perimeter ground shield, PGS

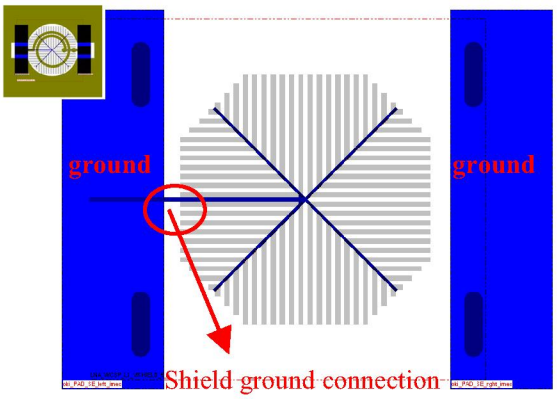



Fig. 4 Center ground shield, CGS

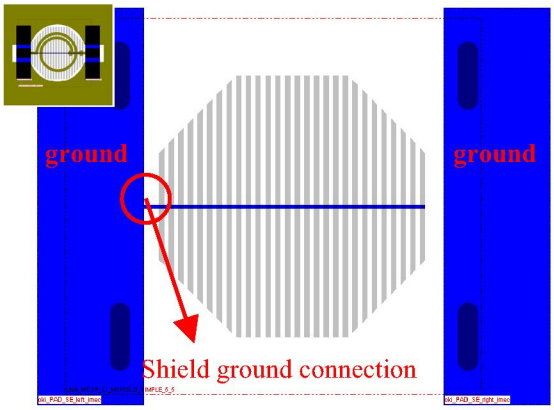



Fig. 5 Simple ground shield, SGS

We can notice that in Fig. 6, Ls7 with PGS is smaller than other inductances Ls3 and Ls5, mainly because the PGS allows an eddy current flow in a direction opposite to that of the current on the spiral; the resulting negative mutual coupling between the currents reduces the magnetic field, and thus the overall inductance Ls7.

$$L = -imag(Y_{21})/\omega \qquad (1)$$

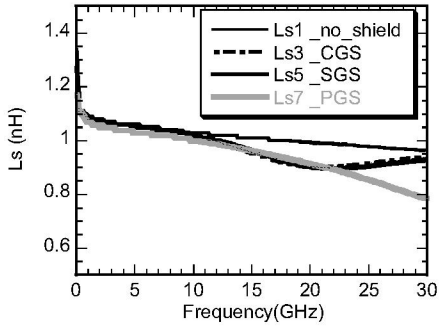



Fig. 6. Measured inductance values w/o shield: Ls1 without shield; Ls3 with center shield; Ls5 with simple shield; Ls7 with perimeter shield; (1μm width and 1μm spacing of shield bars)

The Q-factors have been extracted using the following formulae (2),

$$Q_1 = imag\left(\frac{1}{Y_{11}}\right) \Big/ real\left(\frac{1}{Y_{11}}\right) \qquad (2)$$

$$Q_2 = imag\left(\frac{1}{Y_{22}}\right) \Big/ real\left(\frac{1}{Y_{22}}\right)$$

From Fig. 7, we can conclude that PGS do not improve the inductor $Q_{max}$ [4] due to the small Ls, but CGS and SGS improve significantly the inductor performance. Since CGS and SGS do give the same performance, we can replace CGS by SGS version by obtaining simplified structure.

It can also be noticed that Q6 (extracted from port1) is better than Q5 (extracted from port2) for SGS case; also Q4 (extracted from port1) is better than Q3 (extracted from port2) for CGS case.

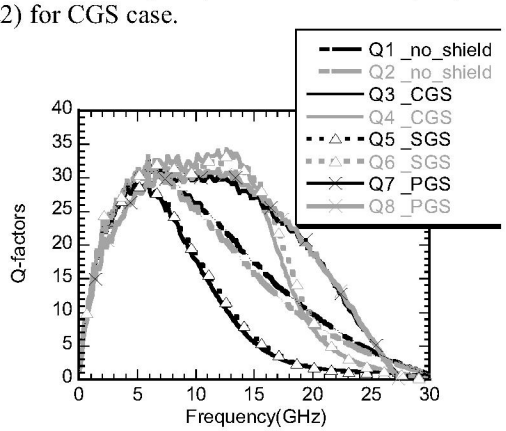



Fig. 7. Measured inductor L2 performance w/o shielQ1, Q2 without shield; Q3, Q4 with center shield; Q5, Q6 with simple grounded shield; Q7, Q8 with perimeter grounded shield; (1μm width and 1μm spacing of shield bars)

We hypothesize that these differences are mainly due to the fact that the shields have been connected only to one side of

RF ground pad instead of double side RF ground pads for CGS (Fig. 4) and SGS case (Fig. 5); this also explains why the Q8/Q7 (Perimeter ground shield) have the same Q-factors since they are connected to double RF ground pad.

To verify our hypotheses, Ansoft HFSS simulations have been performed on inductor L2 with simple ground shield (SGS). Since the shields bars with very small dimensions are difficult to simulate (memory requirement, time) in Ansoft HFSS, and shields with larger dimensions can be more easily simulated, it makes sense to do so when the performance of shields with larger dimensions is known and comparable to shields with smaller dimensions. In order to reduce memory requirements for the simulations, the shield bars width and spacing have been set to 10μm in our simulation.

### *A. SGS Shields with single side RF ground pad connection*

Fig. 8 shows a good agreement between HFSS simulations and measurements for shields with single side RF ground pad connection as in Fig. 5. The agreement verifies that the difference between the Q1/Q2 from port1 and port2 arises from shields to single sided RF ground pad connections.

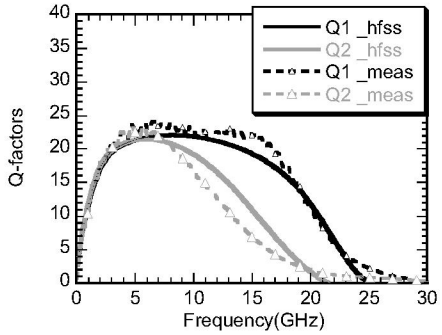
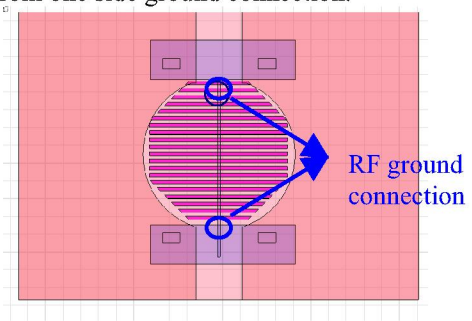



Fig. 8 Inductor L2 combined with Simple shield one side connected to ground (10μm width and 10μm spacing of shield bars), Measurement versus simulation

### *B. SGS Shields with double side RF ground pads connection*

With the same inductor L2, HFSS simulation of shield with double side RF Ground pad connections (Fig. 9) has been performed. The result in Fig. 9 shows that the Q1/Q2 extracted from port1/port2 are equal; also $Q_{max}$ of 32 can be obtained from the double-sided ground connection instead of $Q_{max}$ 24 from one side ground connection.



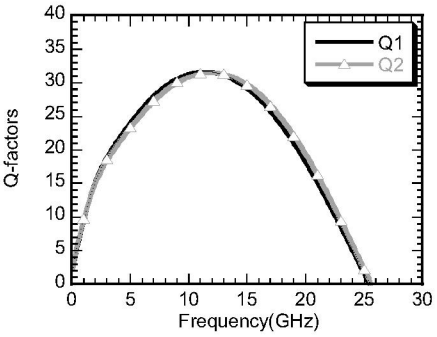




Fig. 9 HFSS simulations of inductor with SGS double side connections to ground (10μm width and 10μm spacing of shield bars)

Hence shield with double side ground pad connection is the optimized structure for improving single-ended inductor performances.

## IV. Influence of Shield Bars Width and Spacing on Inductor Performance

To investigate the effect of shield layout, shield bars with different strip width (1, 5 and 10 um) and spacing (1, 5 and 10 um) are fabricated, keeping the width to spacing ratio equal to one another, so that the same shield density is obtained. Best performance is expected for the smallest shield dimensions, as eddy currents generated in the shield will be smallest. Fig. 10 verifies that the inductor with 1μm strip width and spacing has the best performance with a $Q_{max}$ of 35; Q-factor decreases from 35 to 25 as bars width and gap increase from 1 um to 10 um. So the 5 um and 10 um shields do not improve the $Q_{max}$ of the inductor, but the 1 um shield improves the inductor performance. This means the spacing should be sufficiently narrow so that the vertical electrical field cannot leak through the patterned ground into the underlying silicon substrate [5].

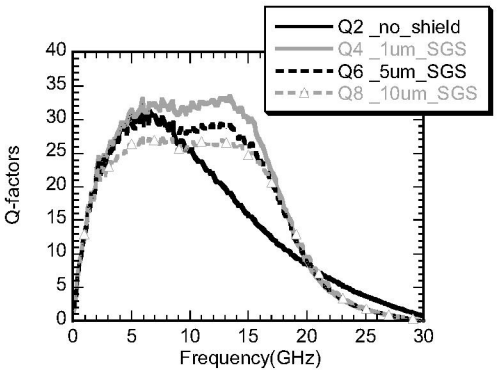
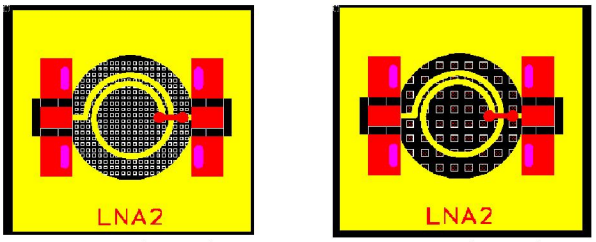



Fig. 11 Measured Q-factors of inductor with/without simple shield (SGS, shield bars and spacing width: 1 um, 5 um and 10um separately)

## V. Effects of Dummy Metals on Inductors

Dummy metals may be required underneath WLP inductor for CMP reasons [6]. Hence, in this section we want to assess the influence of dummies on the above-IC inductor performance (Fig. 12).




10µm width/length/gap 25µm width/length/gap

Fig. 12 Inductor with different dummy dimensions below

We notice from the measurements (Fig. 13) that the inductor without dummy metals below has the best performance; and inductor combined with 10µm wide 10µm long dummy has a better performance than 25µm wide 25µm long dummy metals. Lowest impact on inductor performance is obtained from smallest dummy dimensions.

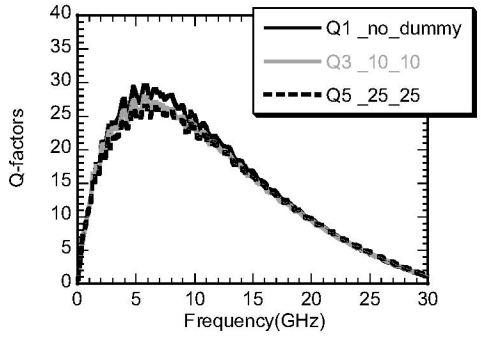



Fig. 13. Measured influence of dummy metal dimensions below inductor: Q1 without dummy; Q3 with 10µm_10µm dummy metal; Q5 with 25µm_25µm dummy metal

## VI. Conclusion

The effects of BEOL M4 patterned ground shield configurations on above-IC inductors have been investigated. Firstly, a better inductor performance can be achieved by a symmetric connection of the shield to RF ground. Furthermore, SGS and CGS both improve inductor performance; CGS can be replaced by SGS for obtaining simplified structure. We have also demonstrated that the shield spacing should be as small as possible to improve the inductor performance. Finally we have demonstrated that smaller dummy dimensions have less negative impact on inductor performance compared to large dummy dimension, but the overall impact of dummy dimensions on inductor performance is limited.

## REFERENCES


[1] G. Carchon et al., "Wafer Level Packaging Technology for Low-Loss On-chip Transmission Lines and Inductors," PP.167-168. International Microelectronics and packaging Society 2003 (*IMAPS 2003)*, Boston, MA, November 16-20, 2003.

[2] X. Sun et al., "High-Q On-chip Inductors using Thin- Film Wafer Level Packaging Technology Demonstrated on a 90nm RF-CMOS 5GHz VCO", *35th EUMW*, OCT. 2005. pp. 77-80.

[3] G. Carchon et al., " Thin-Film as Enabling Passive Integration Technology for RF SoC and SiP", *2005 IEEE International Solid-State Circuit Conference (ISSCC)*, pp.398-399, San Francisco, February 6-10, 2005

[4] L. F. Tiemeijer et al., "Record Q symmetrical inductors for 10-GHz LC-VCOs in 0.18-µm gate-length CMOS," *IEEE Electron Device Letters,* vol. 23, no. 12, pp. 713-715, December 2002.

[5] C. P. Yue et al., " On-chip spiral inductors with patterned ground shields for Si-based RFIC's ," *IEEE J. Solid-state Circuit,* vol.33, pp.743-752, May 1998.

[6] C.Detcheverry et al., "The effect of copper design on inductor performance", *ESSDERC,* Sept. 2003, pp.107-110